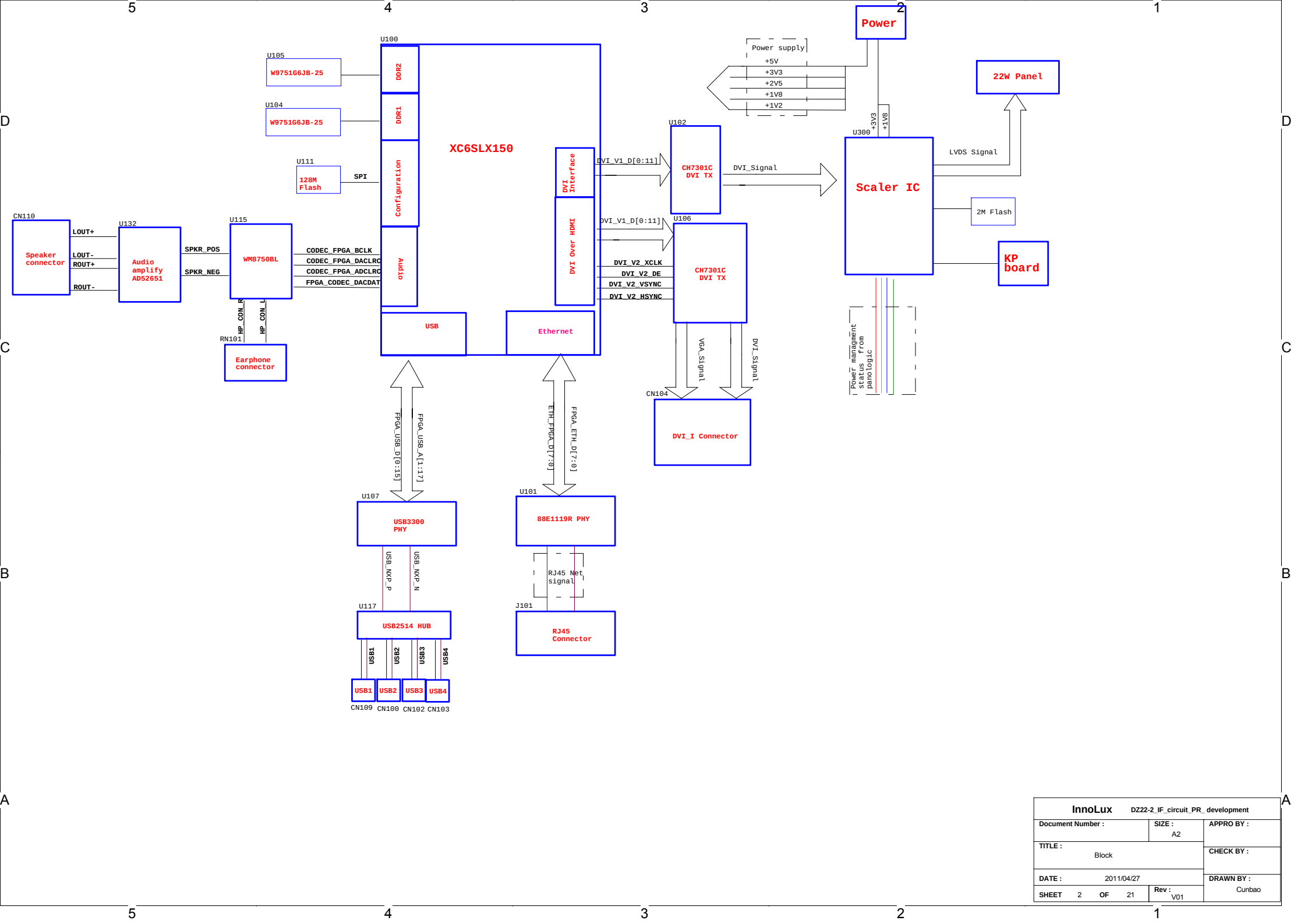
Project Name	DZ22-2 Interface Board Schematic

CONTENTS

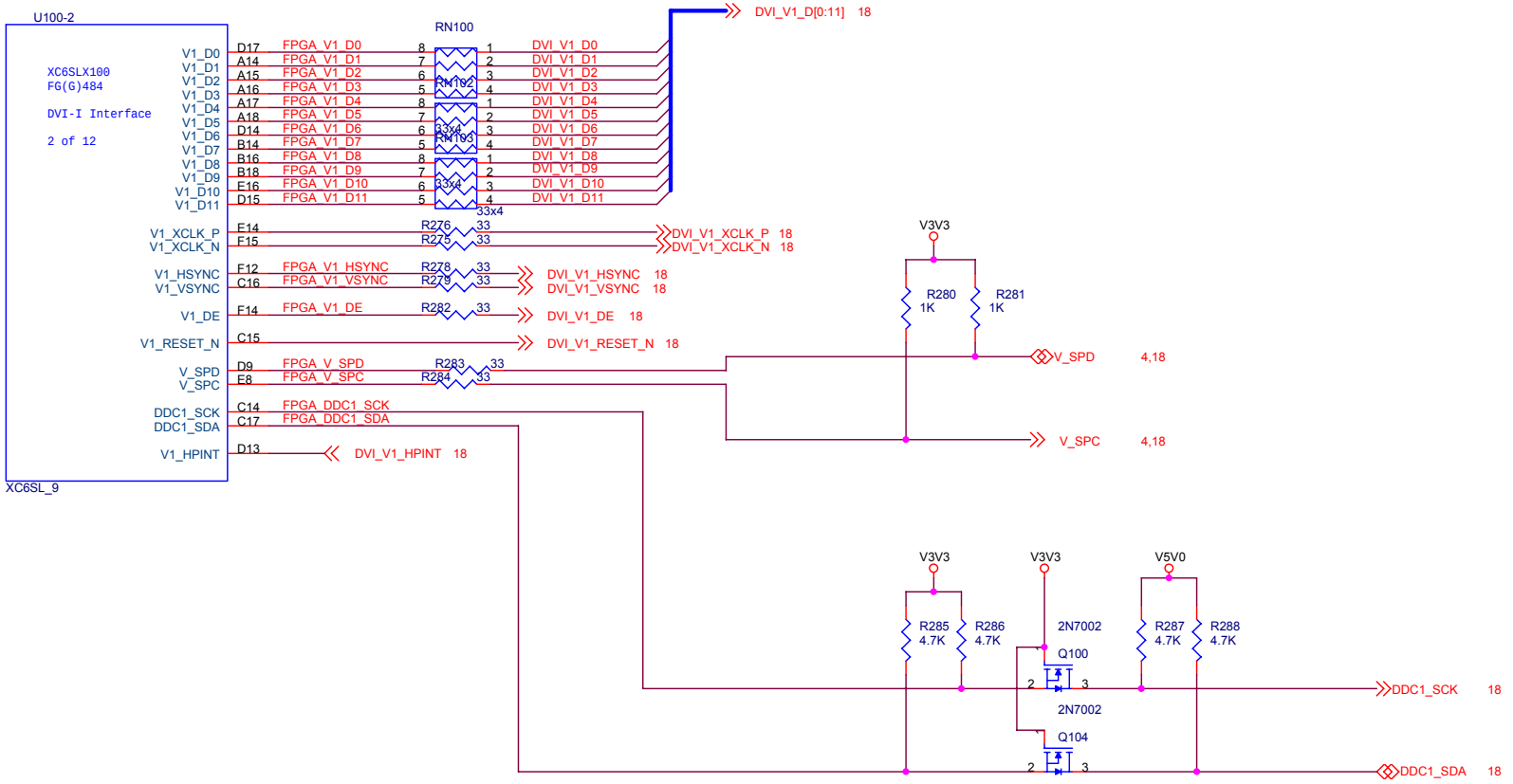
REVISION HISTORY

Date	Author	Version	Comments	Remark
2010/07/10	Cunbao	V01	First edition release for EVT	
2010/09/29	Cunbao	V01	DVT modify:add power mangment function	
2010/12/06	Cunbao	V01	PVT add current limted resistor R328--- P19,add R484,R485,R486,R487 for EMI issue.	
2010/12/07	Cunbao	V01	Connect C339 with ground for the VGA output issue,change value R407 for factory test, R423,R422,R424 for keypad LED luminance,add C373 and modify layout for low temperature issue	
2011/01/17	Cunbao	V01	Add CN108 for POE issue,delete R448 R449 R450 R451 for convenient layout about adding the CN108,delete FB131 FB132 for resistor match	
2011/03/08	Cunbao	V01	Add Q206 R488 C569 reserved for Q205 high temperature,add FB107 for ripple voltage,add C116 C118 C225 C561 C562 C563 C564 C565 C566 C567 C568 R223 R224 R230 R231 R223 R224 for DDR signal good performance.	
2011/03/29	Cunbao	V01	DVT II Change IC U132 Vender to AD52651,U104 U105Vender to W9751G6JB-25	
2011/04/27	Cunbao	V01	DeleteR103,R104,R105,R106,R107,R108,R109,R110,R111,R112,R113,R114,R115,R116,R119,R120, R121,R130,R131,R133,R134,R135,R136,R137,R138,R139,R141,R142,R143,R144,R117,R118,R132, R140,R145,R146,R147,R148,same with Panologic design.Add R473~R476 for status stable,NC Q205 delete FB107and add Q206 R488 for 5v low voltage drop.For DVI EMI issue,change FB127~FB130 material and footprint.Reserve C304 R445 for AC ON pulse issue,add C570 C438 to avoid AC ON VCC_5V high current.	

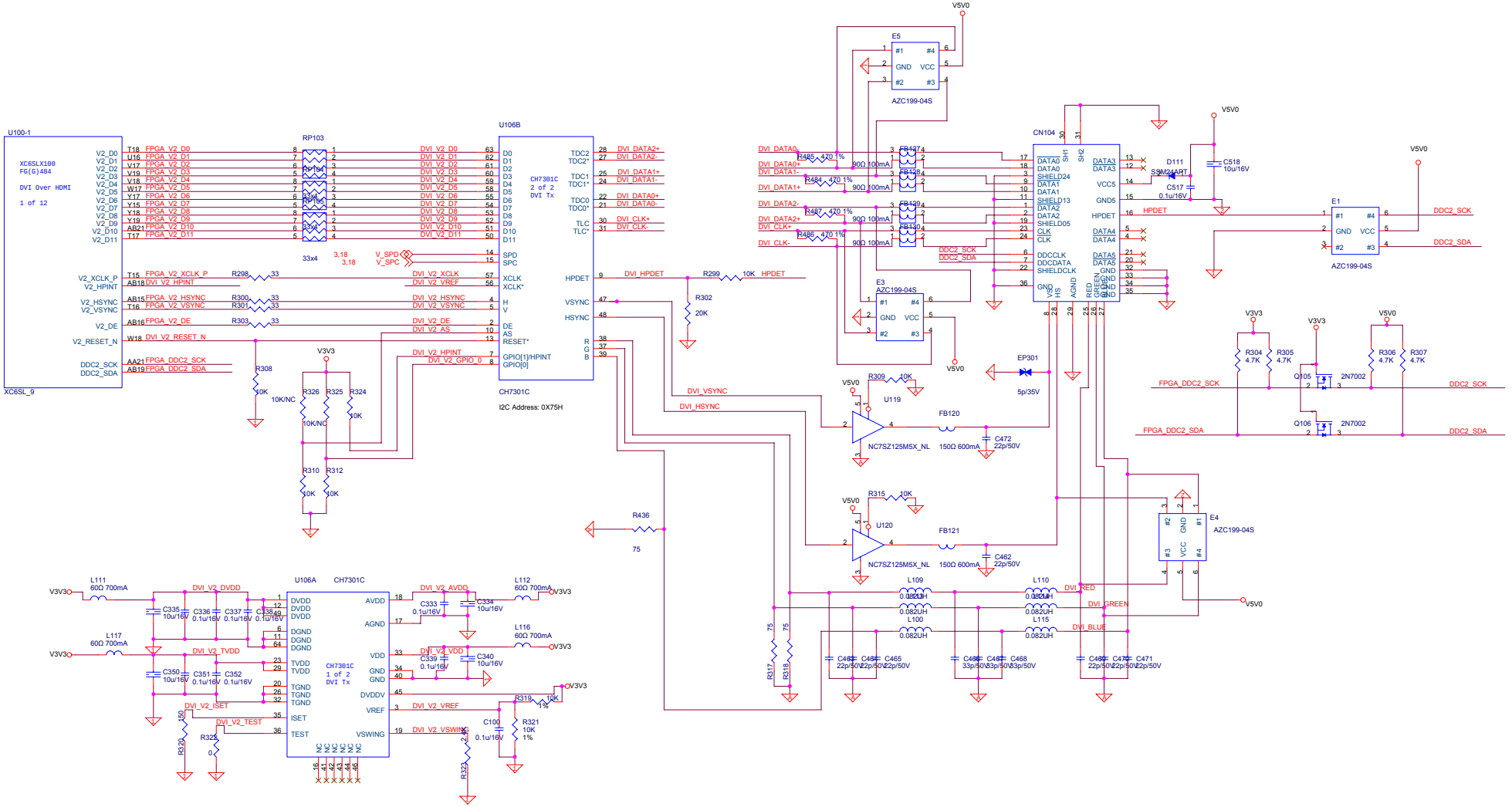
InnoLux	DZ22-2_IF_circuit_PR_ development	
Document Number :	SIZE : A3	APPRO BY :
TITLE : Contents		CHECK BY :
DATE : 2011/04/27		DRAWN BY : Cunbao
SHEET 1 OF 21	Rev : V01	



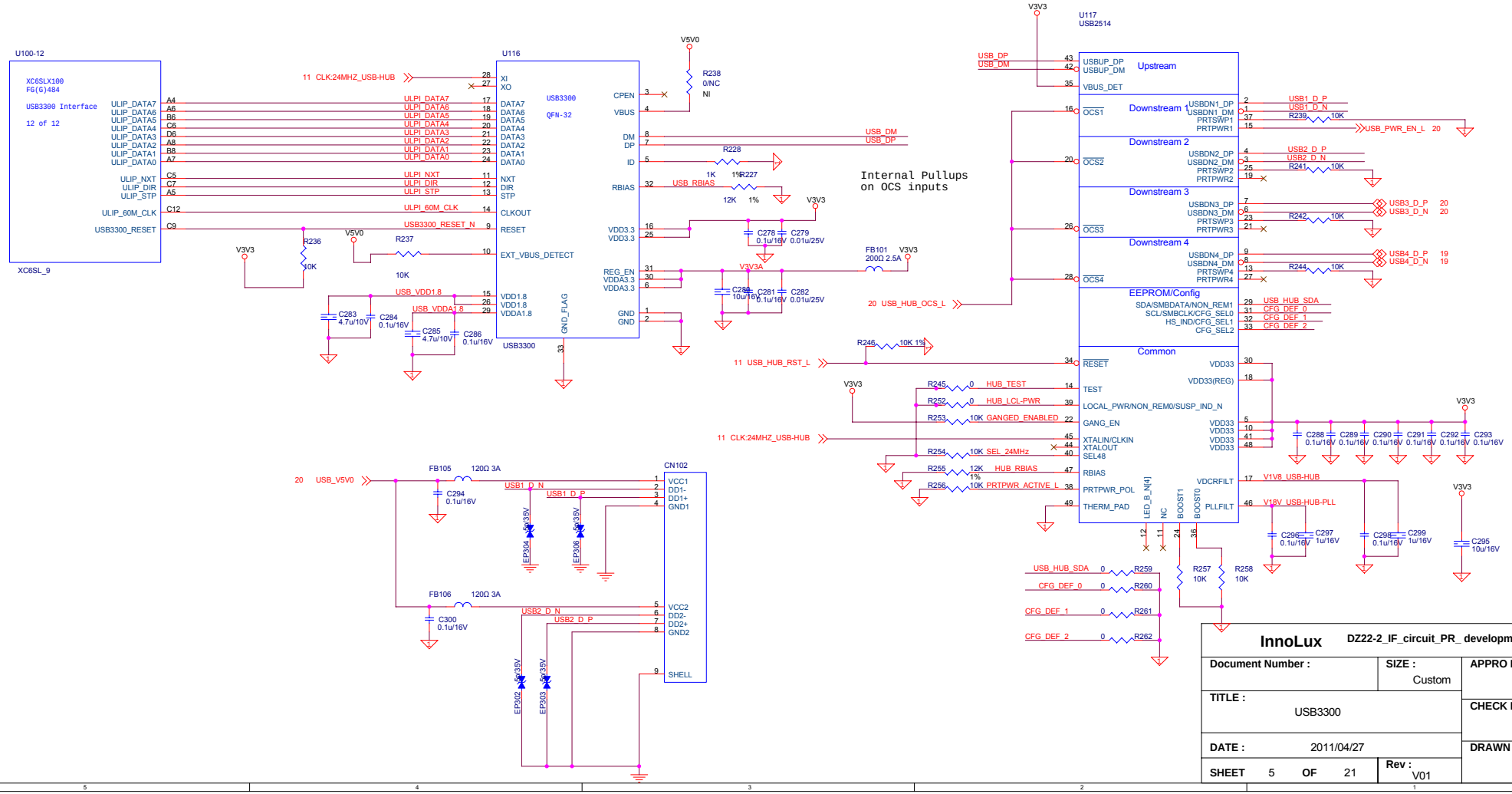
InnoLux	DZ22-2_IF_circuit_PR_ development	
Document Number :	SIZE : A2	APPRO BY :
TITLE : Block		CHECK BY :
DATE : 2011/04/27		DRAWN BY : Cunbao
SHEET 2 OF 21	Rev : V01	

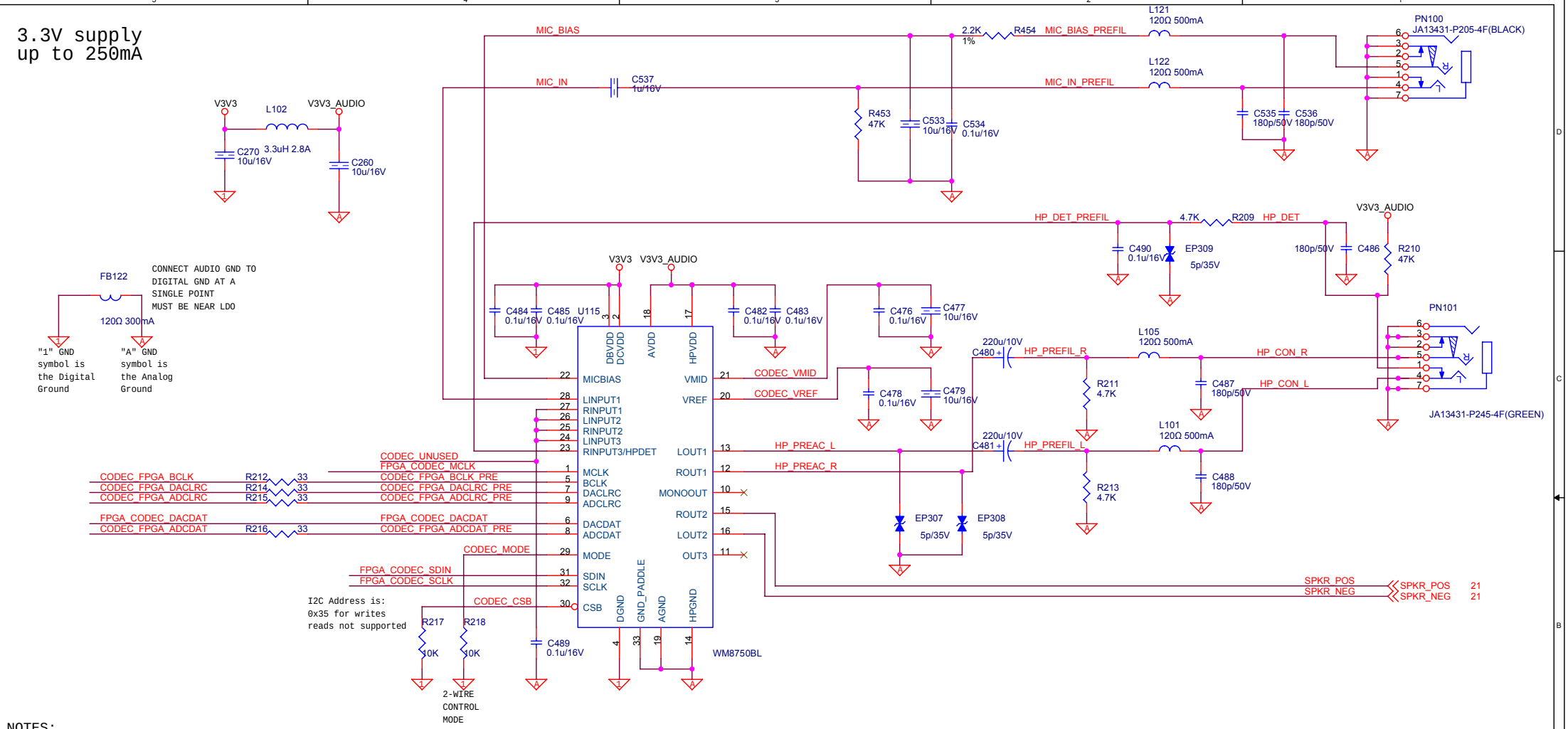


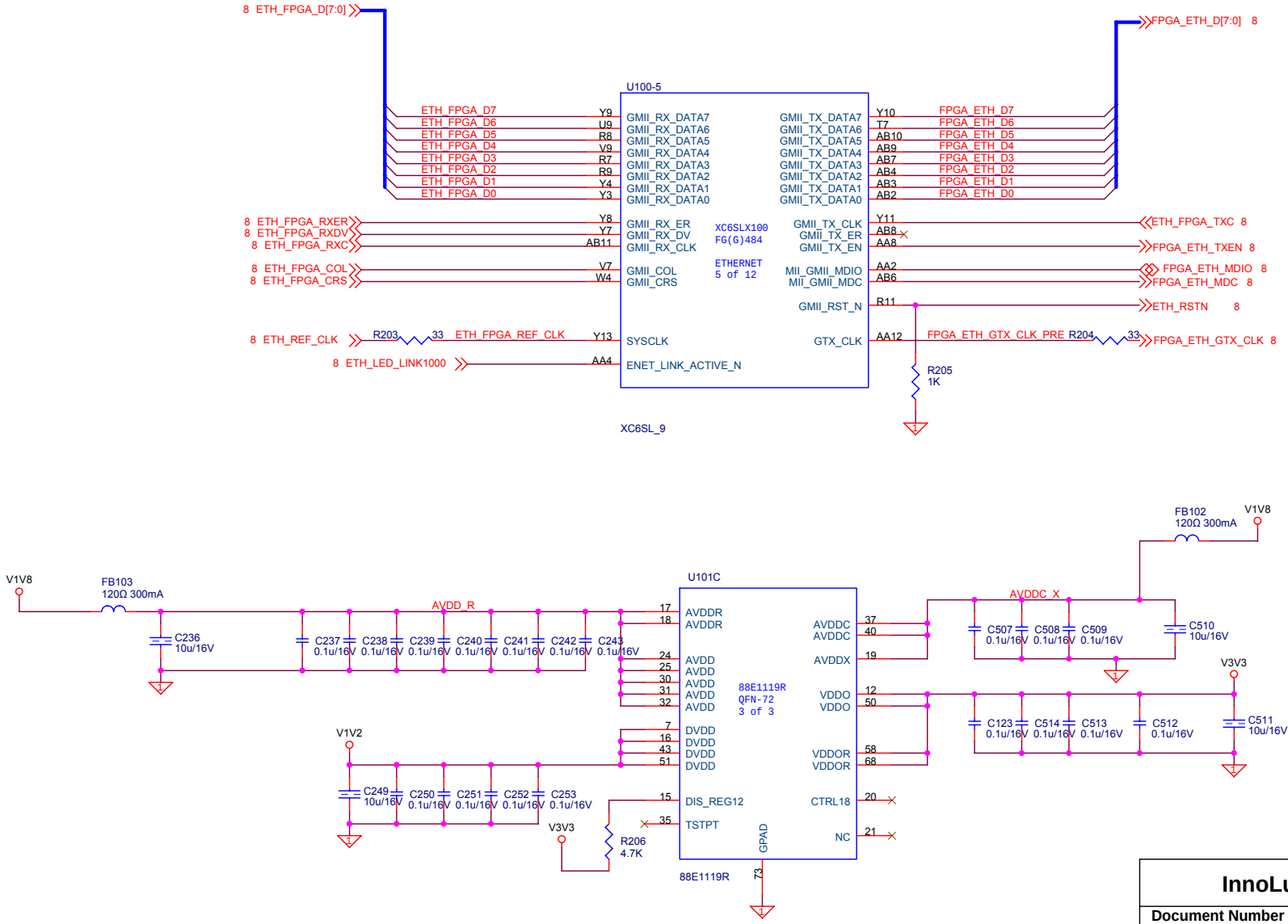
InnoLux DZ22-2_IF_circuit_PR_ development			
Document Number :	**SIZE :** B		**APPRO BY :**
TITLE : DVI-I Interface			**CHECK BY :**
DATE : 2011/04/27			**DRAWN BY :** Cunbao
SHEET 3 **OF** 21	**Rev :** V01		



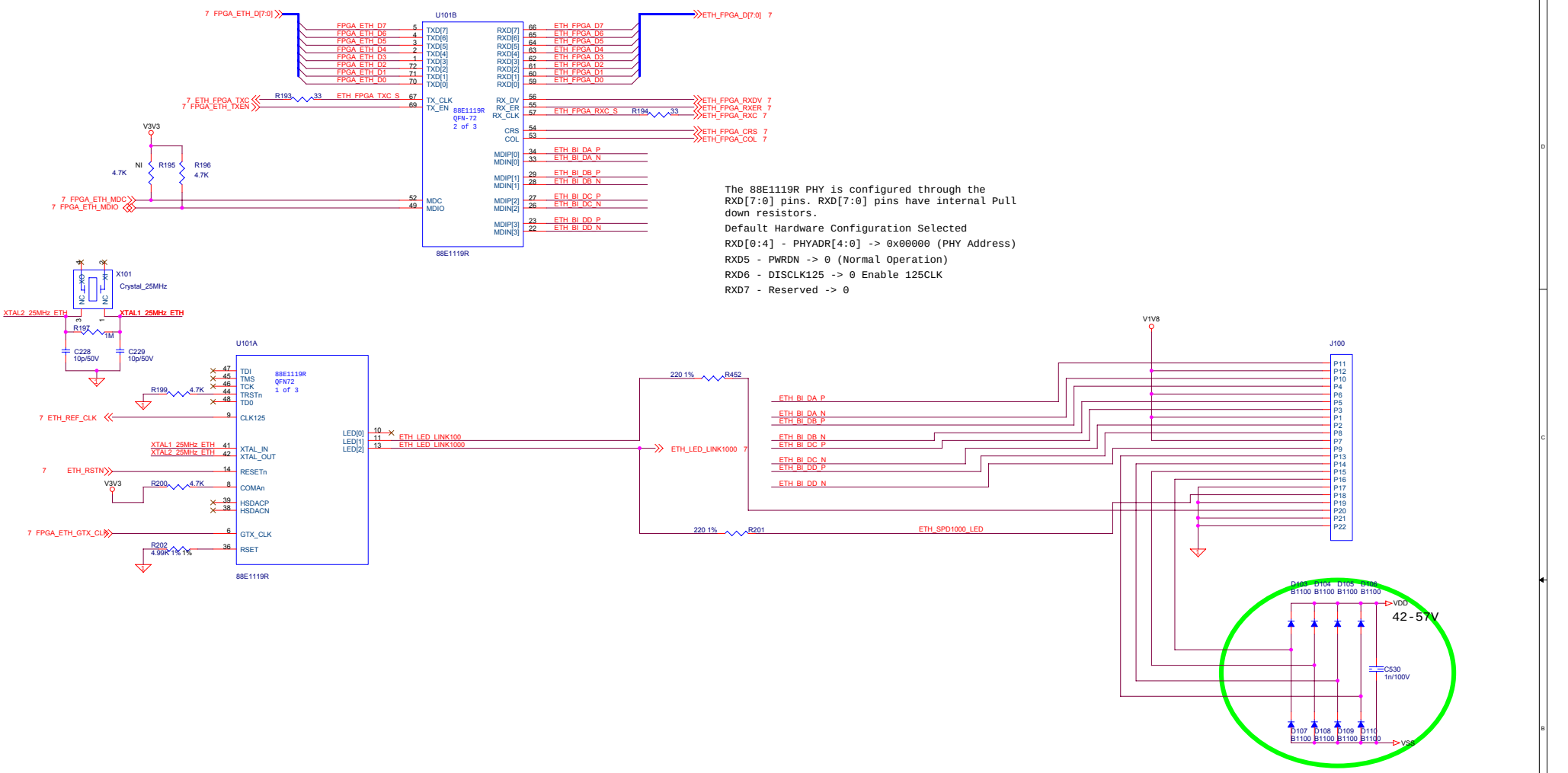
InnoLux	DZ22-2_IF_circuit_PR_ development	
Document Number :	**SIZE :** C	**APPRO BY :**
TITLE : DVI Over HDMI Interface		**CHECK BY :**
DATE : 2011/04/27		**DRAWN BY :** Cunbao
SHEET 4 **OF** 21	**Rev :** V01	


U100-12
XC6SLX100
FG(G)484
USB3300 Interface
12 of 12
XC6SL_9
U116
USB3300
QFN-32
11 CLK:24MHZ_USB-HUB
ULPI_DATA7
ULPI_DATA6
ULPI_DATA5
ULPI_DATA4
ULPI_DATA3
ULPI_DATA2
ULPI_DATA1
ULPI_DATA0
ULPI_NXT
ULPI_DIR
ULPI_STP
ULPI_60M_CLK
USB3300_RESET
USB3300_RESET_N
EXT_VBUS_DETECT
GND_FLAG
V5V0
V3V3
V3V3A
R238 0/NC NI
R228
R227
USB_RBIAS
FB101 200Ω 2.5A
20 USB_HUB_OCS_L
Internal Pullups on OCS inputs
U117
USB2514
Upstream
Downstream 1
Downstream 2
Downstream 3
Downstream 4
EEPROM/Config
Common
USB_DP
USB_DM
USB1_D_P
USB1_D_N
USB2_D_P
USB2_D_N
USB3_D_P
USB3_D_N
USB4_D_P
USB4_D_N
USB_PWR_EN_L
USB_HUB_SDA
CFG_DEF_0
CFG_DEF_1
CFG_DEF_2
11 USB_HUB_RST_L
R246 10K 1%
HUB_TEST
HUB_LCL-PWR
10K GANGED_ENABLED
11 CLK:24MHZ_USB-HUB
10K SEL_24MHz
12K HUB_RBIAS
10K PRTPWR_ACTIVE_L
V1V8_USB-HUB
V1V8_USB-HUB-PLL
20 USB_V5V0
FB105 120Ω 3A
FB106 120Ω 3A
CN102
VCC1
DD1-
DD1+
GND1
VCC2
DD2-
DD2+
GND2
SHELL
EP304
EP306
EP302
EP303
InnoLux
DZ22-2_IF_circuit_PR_ development
Document Number :
SIZE : Custom
APPRO BY :
TITLE : USB3300
CHECK BY :
DATE : 2011/04/27
DRAWN BY : Cunbao
SHEET 5 OF 21
Rev : V01


3.3V supply
up to 250mA
V3V3
L102
V3V3_AUDIO
C270 10u/16V
3.3uH 2.8A
C260 10u/16V
MIC_BIAS
MIC_IN
C537 1u/16V
2.2K 1%
R454
MIC_BIAS_PREFIL
L121 120Ω 500mA
L122 120Ω 500mA
MIC_IN_PREFIL
R453 47K
C533 10u/16V
C534 0.1u/16V
C535 180p/50V
C536 180p/50V
PN100
JA13431-P205-4F(BLACK)
HP_DET_PREFIL
4.7K
R209
HP_DET
C490 0.1u/16V
EP309 5p/35V
180p/50V
C486
R210 47K
FB122
120Ω 300mA
CONNECT AUDIO GND TO
DIGITAL GND AT A
SINGLE POINT
MUST BE NEAR LDO
"1" GND
symbol is
the Digital
Ground
"A" GND
symbol is
the Analog
Ground
C484 0.1u/16V
C485 0.1u/16V
U115
C482 0.1u/16V
C483 0.1u/16V
C476 0.1u/16V
C477 10u/16V
C478 0.1u/16V
C479 10u/16V
DBVDD
DCVDD
AVDD
HPVDD
MICBIAS
VMID
VREF
LINPUT1
RINPUT1
LINPUT2
RINPUT2
LINPUT3
RINPUT3/HPDET
LOUT1
ROUT1
MONOOUT
ROUT2
LOUT2
OUT3
MCLK
BCLK
DACLRC
ADCLRC
DACDAT
ADCDAT
MODE
SDIN
SCLK
CSB
DGND
GND_PADDLE
AGND
HPGND
CODEC_VMID
CODEC_VREF
CODEC_UNUSED
FPGA_CODEC_MCLK
CODEC_FPGA_BCLK
CODEC_FPGA_DACLRC
CODEC_FPGA_ADCLRC
FPGA_CODEC_DACDAT
CODEC_FPGA_ADCDAT
CODEC_MODE
FPGA_CODEC_SDIN
FPGA_CODEC_SCLK
CODEC_CSB
R212 33
R214 33
R215 33
R216 33
CODEC_FPGA_BCLK_PRE
CODEC_FPGA_DACLRC_PRE
CODEC_FPGA_ADCLRC_PRE
CODEC_FPGA_DACDAT_PRE
I2C Address is:
0x35 for writes
reads not supported
R217 10K
R218 10K
C489 0.1u/16V
2-WIRE
CONTROL
MODE
WM8750BL
220u/10V
C480
HP_PREFIL_R
HP_PREAC_L
HP_PREAC_R
HP_PREFIL_L
220u/10V
C481
R211 4.7K
R213 4.7K
L105 120Ω 500mA
L101 120Ω 500mA
C487 180p/50V
C488 180p/50V
HP_CON_R
HP_CON_L
PN101
JA13431-P245-4F(GREEN)
EP307 5p/35V
EP308 5p/35V
SPKR_POS
SPKR_NEG
SPKR_POS 21
SPKR_NEG 21
NOTES:
1. Layout: Read Power Supply notes on page 46 of WM8750BL data sheet and refer to notes for Figure 50.
2. HPSWEN bit should be set to a 1 HPSWPOL bit should be set to 0.
3. 220uF caps should be 6.3V Aluminum Electrolytics.
U100-4
XC6SLX100
FG(G)484
AUDIO
4 of 12
ADC_BCLK
ADC_ADCLRC
ADC_ADCDAT
ADC_DACLRC
ADC_DACDAT
ADC_MCLK
ADC_SCLK
ADC_SDIN
XC6SL_9
AB13
W9
R13
U6
Y14
W14
U17
AB17
R219 4.7K
R220 4.7K
FPGA_CODEC_DACDAT_S
FPGA_CODEC_MCLK_S
R221 33
R222 33
InnoLux
DZ22-2_IF_circuit_PR_ development
Document Number :
SIZE : B
APPRO BY :
TITLE : Audio Interface
CHECK BY :
DATE : 2011/04/27
DRAWN BY : Cunbao
SHEET 6 OF 21
Rev : V01



InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** B	**APPRO BY :**
TITLE :	PGA Ethernet Interface		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 7	**OF** 21	**Rev :** V01	

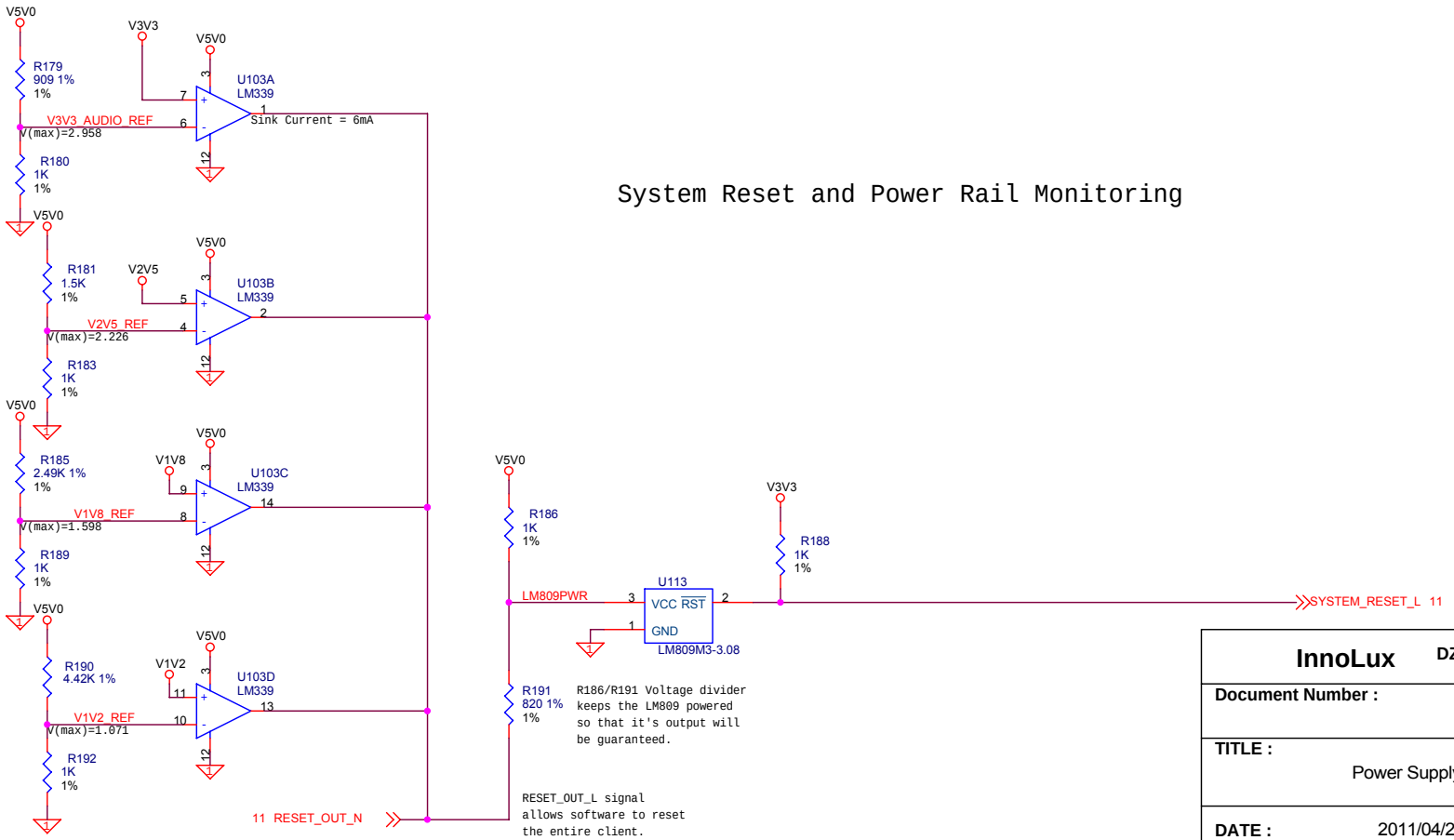


For DZ19-2 mode, delete these componment

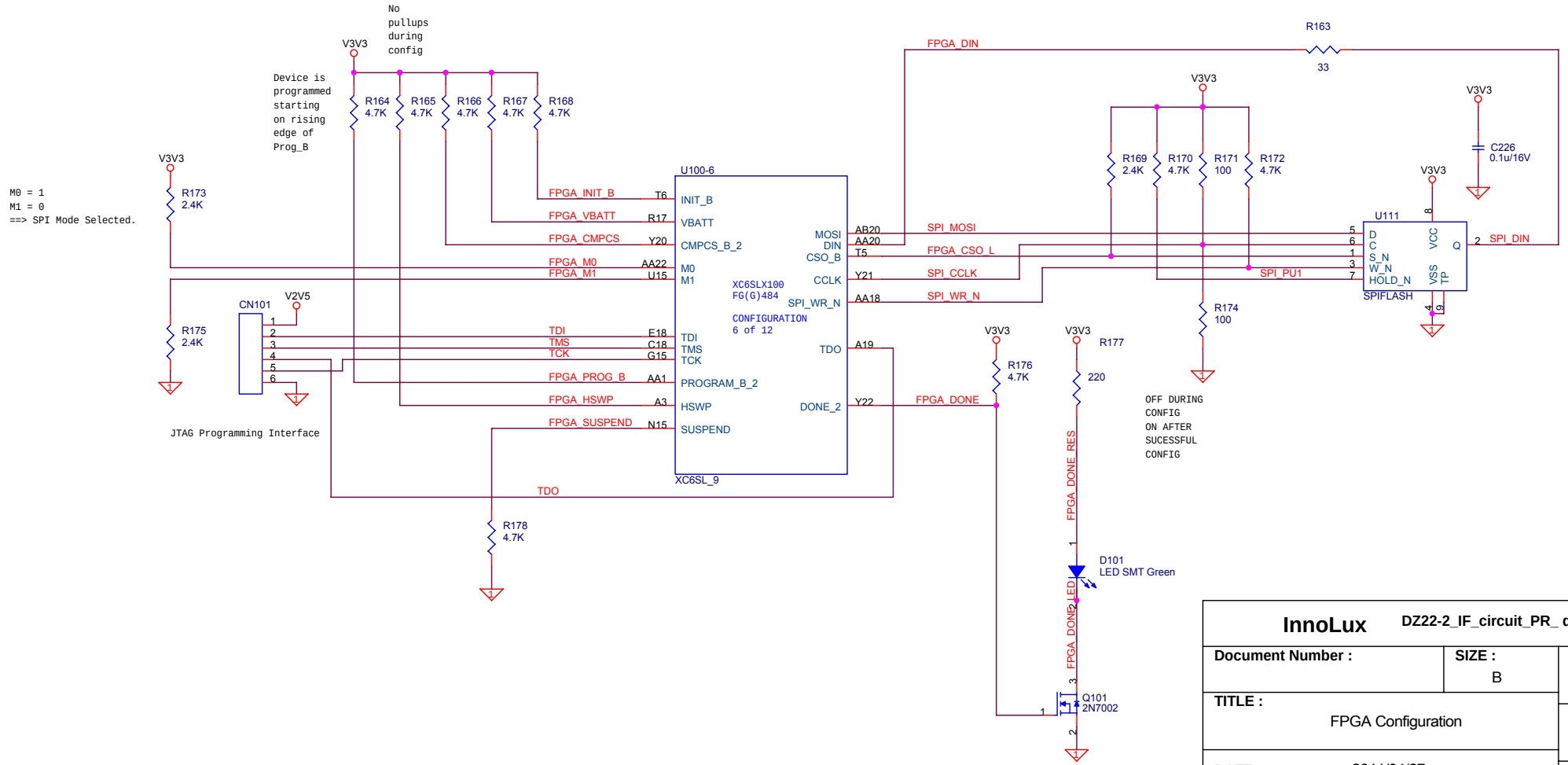
InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** C	**APPRO BY :**
TITLE :	Ethernet Phy & Port		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 8 **OF** 21		**Rev :** V01	

Assume Vin is up to 10% high (5.5V), bottom resistor is 1% high and top resistor is 1% low when calculating thresholds. Thresholds are set 5% below nominal voltage.

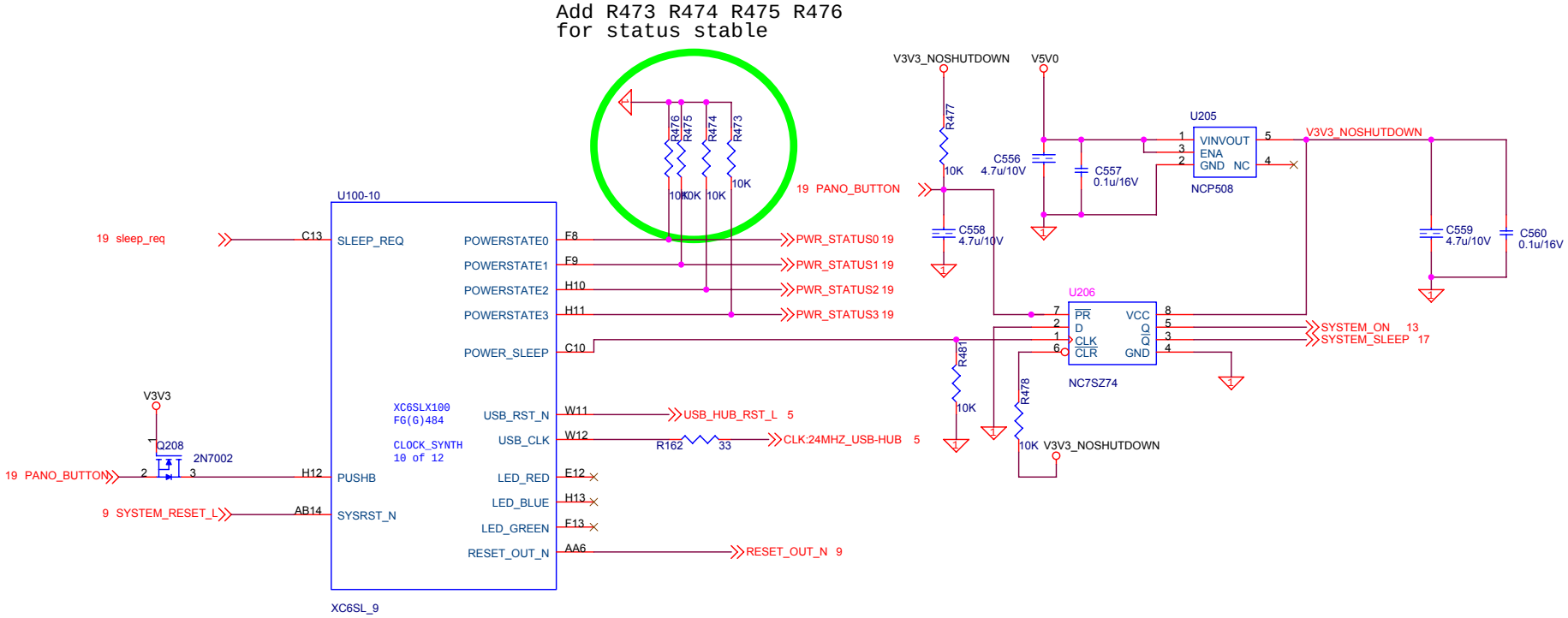
System Reset and Power Rail Monitoring



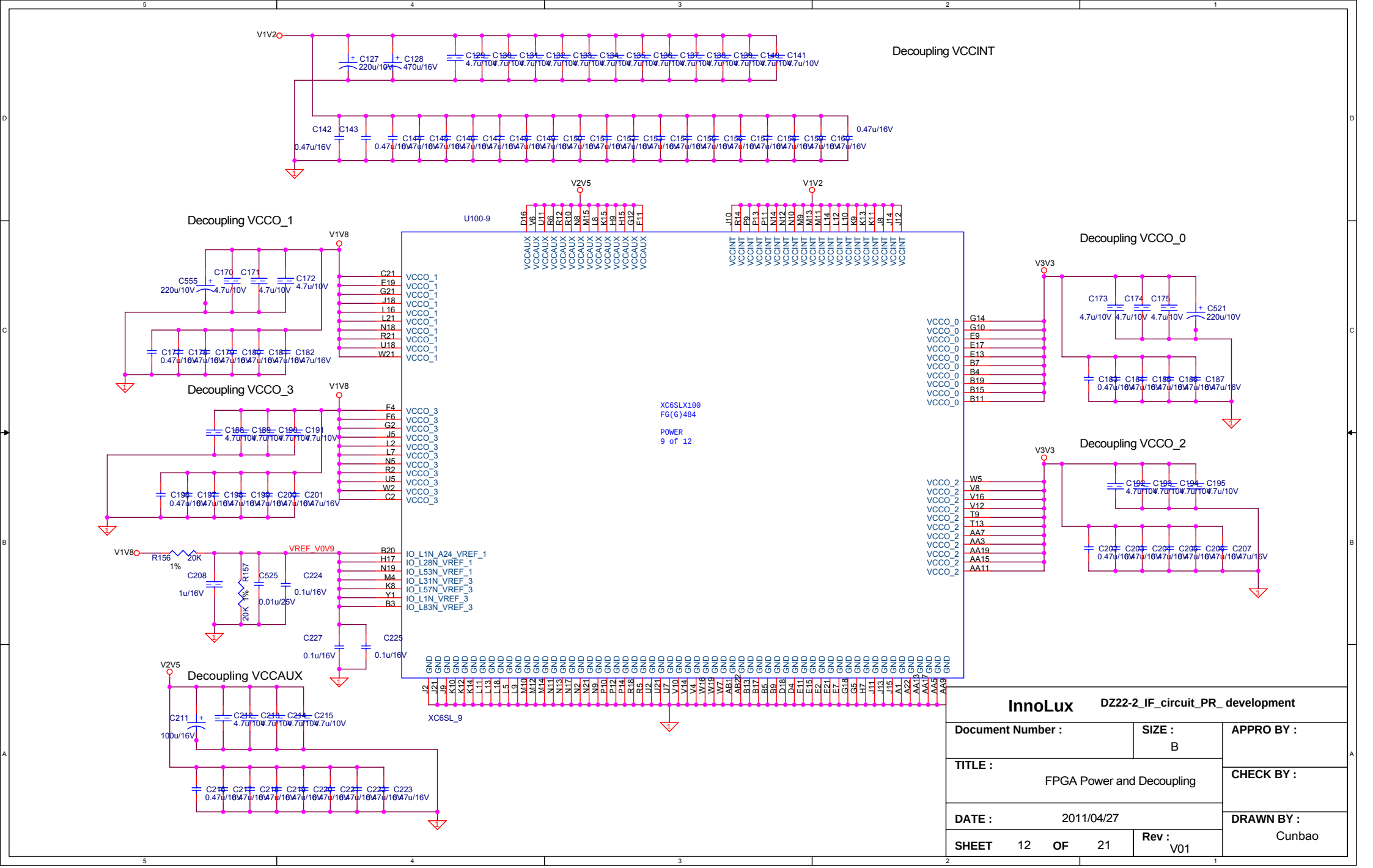
InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** B	**APPRO BY :**
TITLE :	Power Supply Monitoring		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 9 **OF** 21		**Rev :** V01	

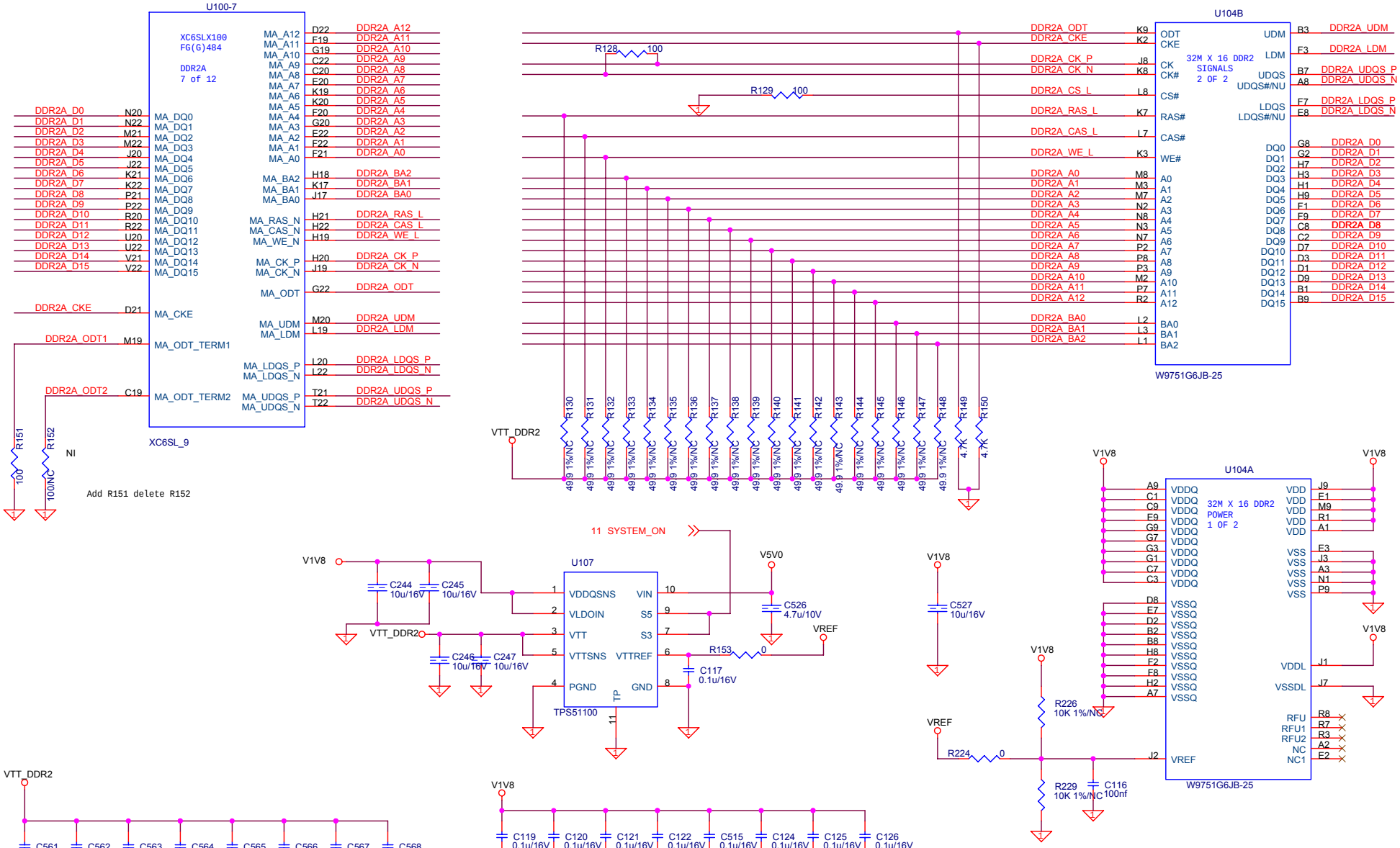


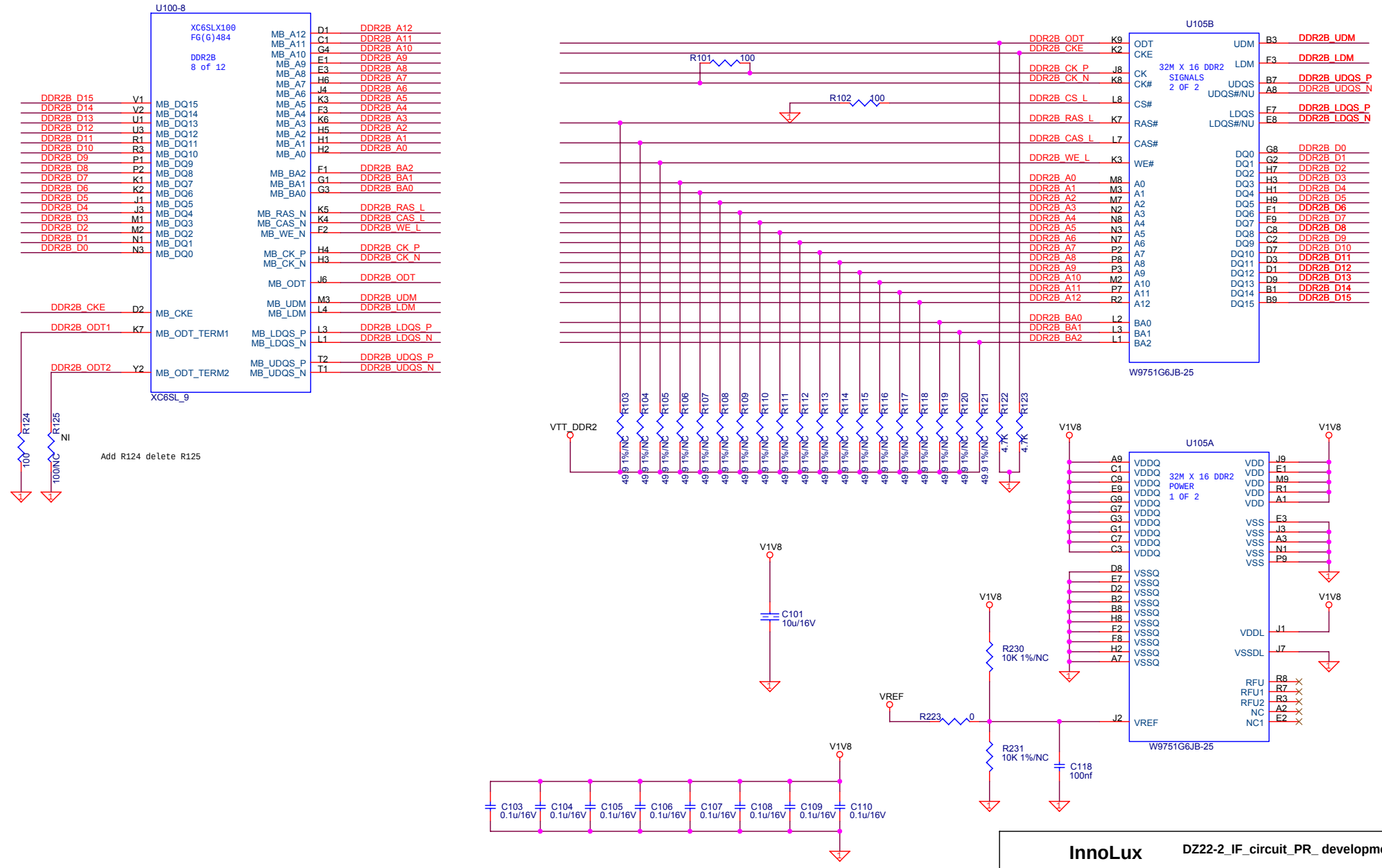
InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** B	**APPRO BY :**
TITLE :	FPGA Configuration		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 10 **OF** 21		**Rev :** V01	



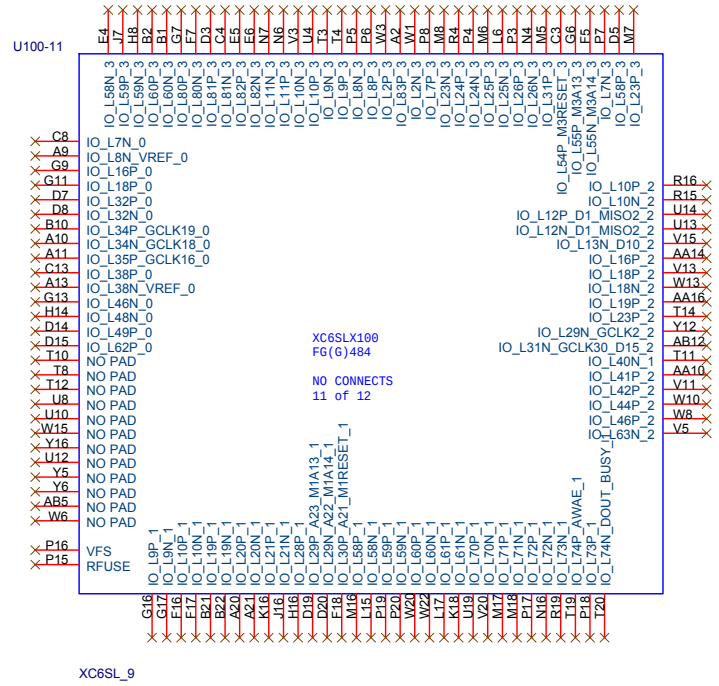
InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** B	**APPRO BY :**
TITLE :	Clock Synthesis		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 11 **OF** 21		**Rev :** V01	


Decoupling VCCINT
Decoupling VCCO_1
Decoupling VCCO_3
Decoupling VCCAUX
Decoupling VCCO_0
Decoupling VCCO_2
U100-9
XC6SLX100
FG(G)484
POWER
9 of 12
XC6SL_9
InnoLux
DZ22-2_IF_circuit_PR_ development
Document Number :
SIZE :
B
APPRO BY :
TITLE :
FPGA Power and Decoupling
CHECK BY :
DATE :
2011/04/27
DRAWN BY :
Cunbao
SHEET 12 OF 21
Rev :
V01

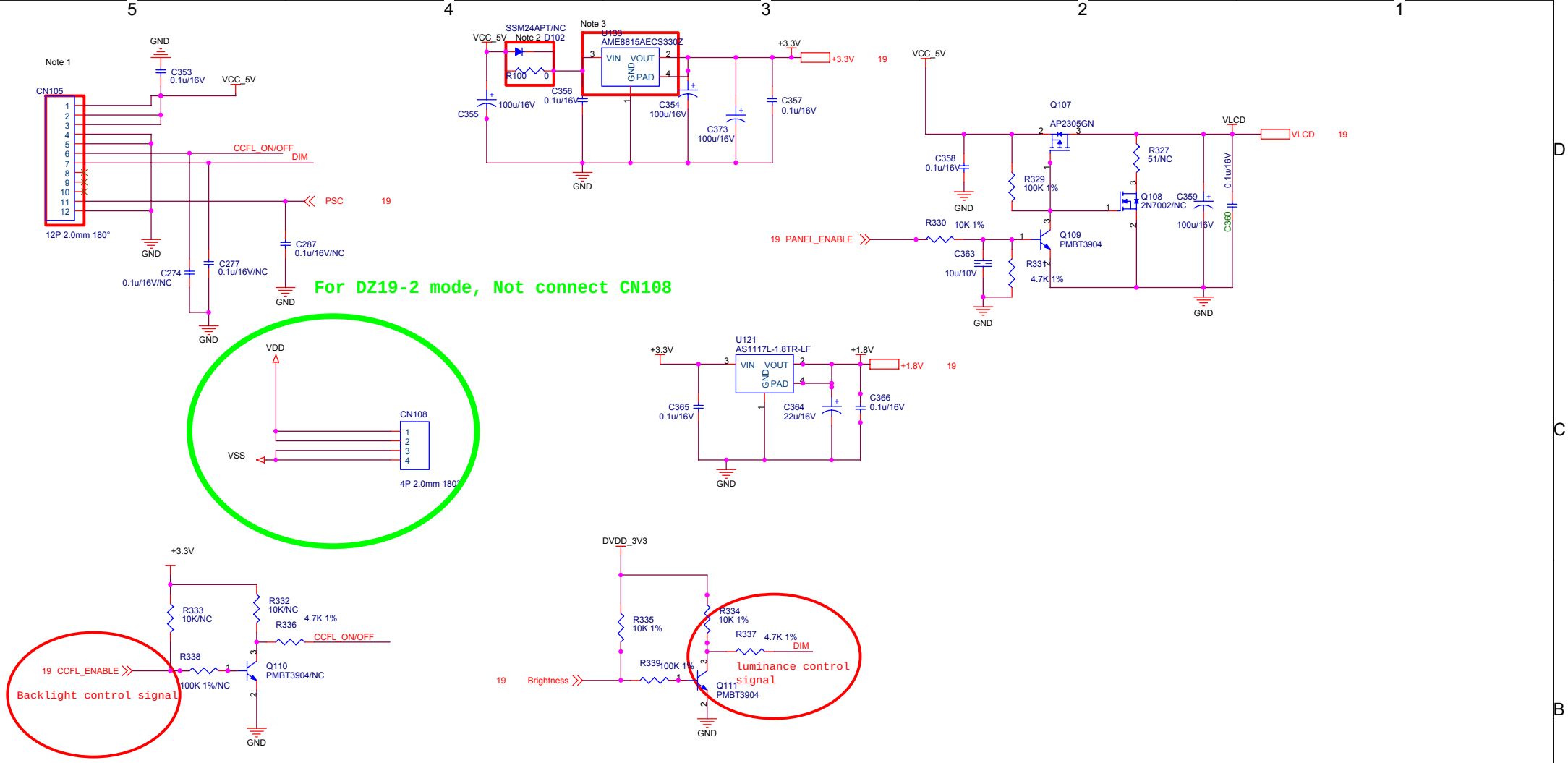

U100-7
XC6SLX100
FG(G)484
DDR2A
7 of 12
XC6SL_9
U104B
W9751G6JB-25
32M X 16 DDR2
SIGNALS
2 OF 2
U104A
32M X 16 DDR2
POWER
1 OF 2
U107
TPS51100
11 SYSTEM_ON
Add R151 delete R152
NI
InnoLux
DZ22-2_IF_circuit_PR_ development
Document Number :
SIZE :
Custom
APPRO BY :
TITLE :
DDR2 SDRAM Interface1
CHECK BY :
DATE :
2011/04/27
DRAWN BY :
Cunbao
SHEET 13 OF 21
Rev :
V01



InnoLux	DZ22-2_IF_circuit_PR_ development	
Document Number :	**SIZE :** Custom	**APPRO BY :**
TITLE : DDR2 SDRAM Interface 2		**CHECK BY :**
DATE : 2011/04/27		**DRAWN BY :** Cunbao
SHEET 14 **OF** 21	**Rev :** V01	

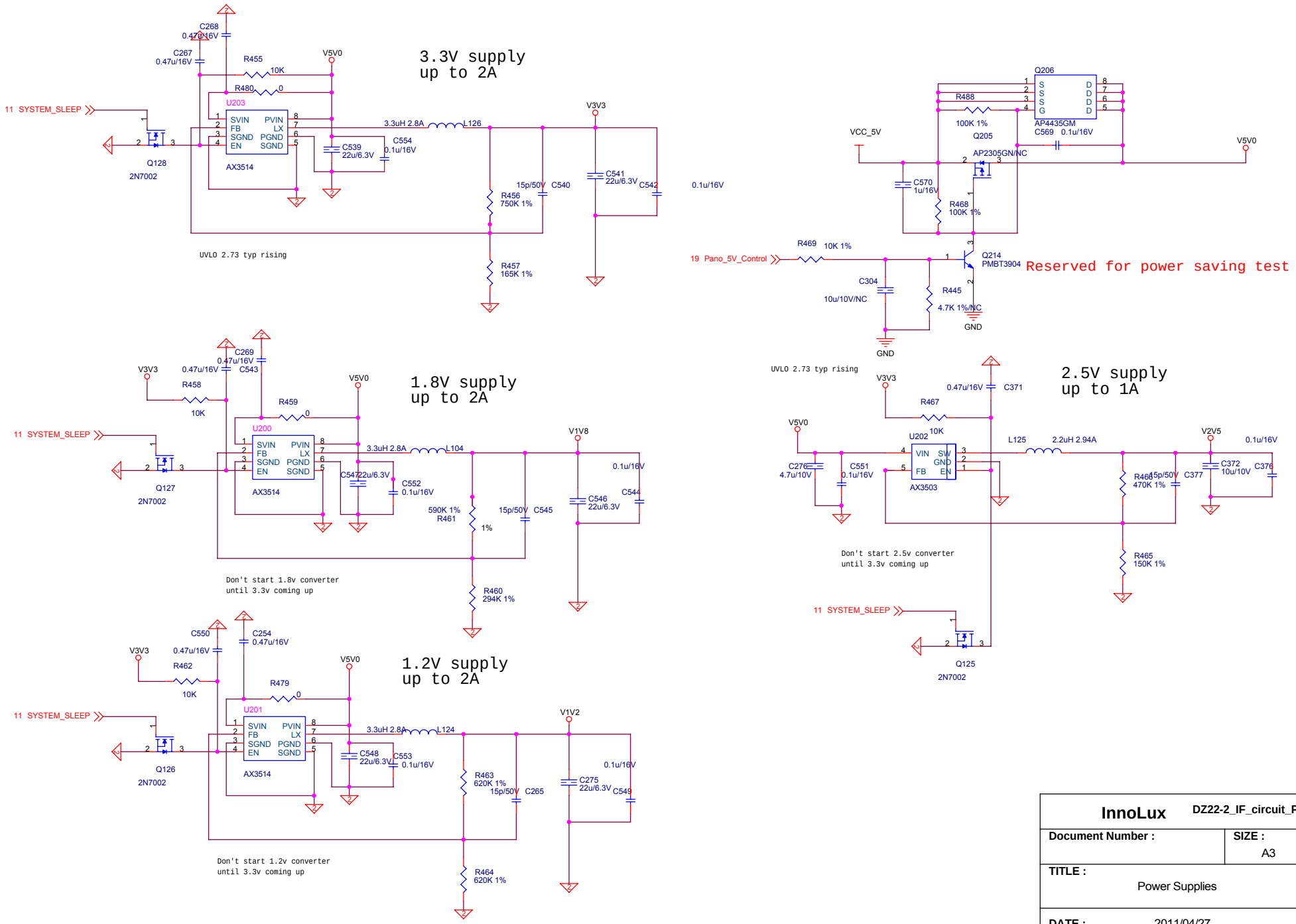


InnoLux	**DZ22-2_IF_circuit_PR_ development**		
Document Number :		**SIZE :** B	**APPRO BY :**
TITLE :	FPGA Debug and No Connect		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 15 **OF** 21		**Rev :** V01	

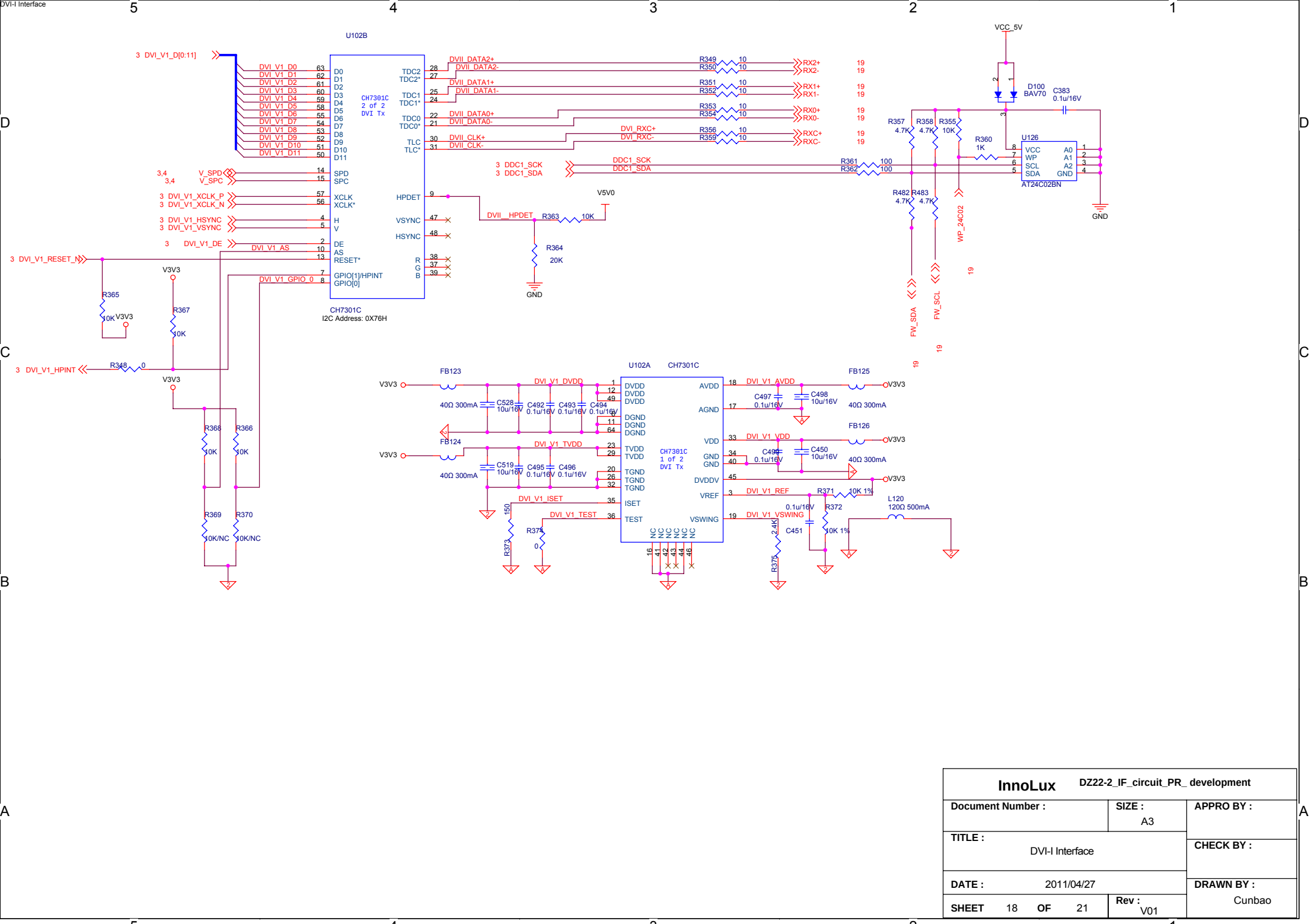


Note:
1. CN101/CN102 is no locked packgae for normal model.CN101 is locked packgae for special model(Dell).
2. D116 must be co-layed with R259
3. U156 must contain TO263, TO252 and SOT223 package

InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** A3	**APPRO BY :**
TITLE :	Monitor-DC-DC		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 16 **OF** 21		**Rev :** V01	



InnoLux	**DZ22-2_IF_circuit_PR_ development**		
Document Number :		**SIZE :** A3	**APPRO BY :**
TITLE : Power Supplies			**CHECK BY :**
DATE : 2011/04/27			**DRAWN BY :** Cunbao
SHEET 17 **OF** 21		**Rev :** EVT	



InnoLux	DZ22-2_IF_circuit_PR_ development		
Document Number :		**SIZE :** A3	**APPRO BY :**
TITLE :	DVI-I Interface		**CHECK BY :**
DATE :	2011/04/27		**DRAWN BY :** Cunbao
SHEET 18 **OF** 21		**Rev :** V01	

Note:
1. Each bypass capacitor (0.1u/16V) must be respectively closed to pin that is DCpower input of scaler IC.
2. Bypass capacitors are for ESD and EMI issue. ESD component EP101,EP102,EP103 are for GPIO direct driving LED.
3. RL401,RL402,RL403,RL404 are reserved for some panel spec.
4. CN403 is no locked packgae for normal model.CN403 is locked packgae for special model(Dell).
5. DIP Connector CN401 for special LVDS input panel

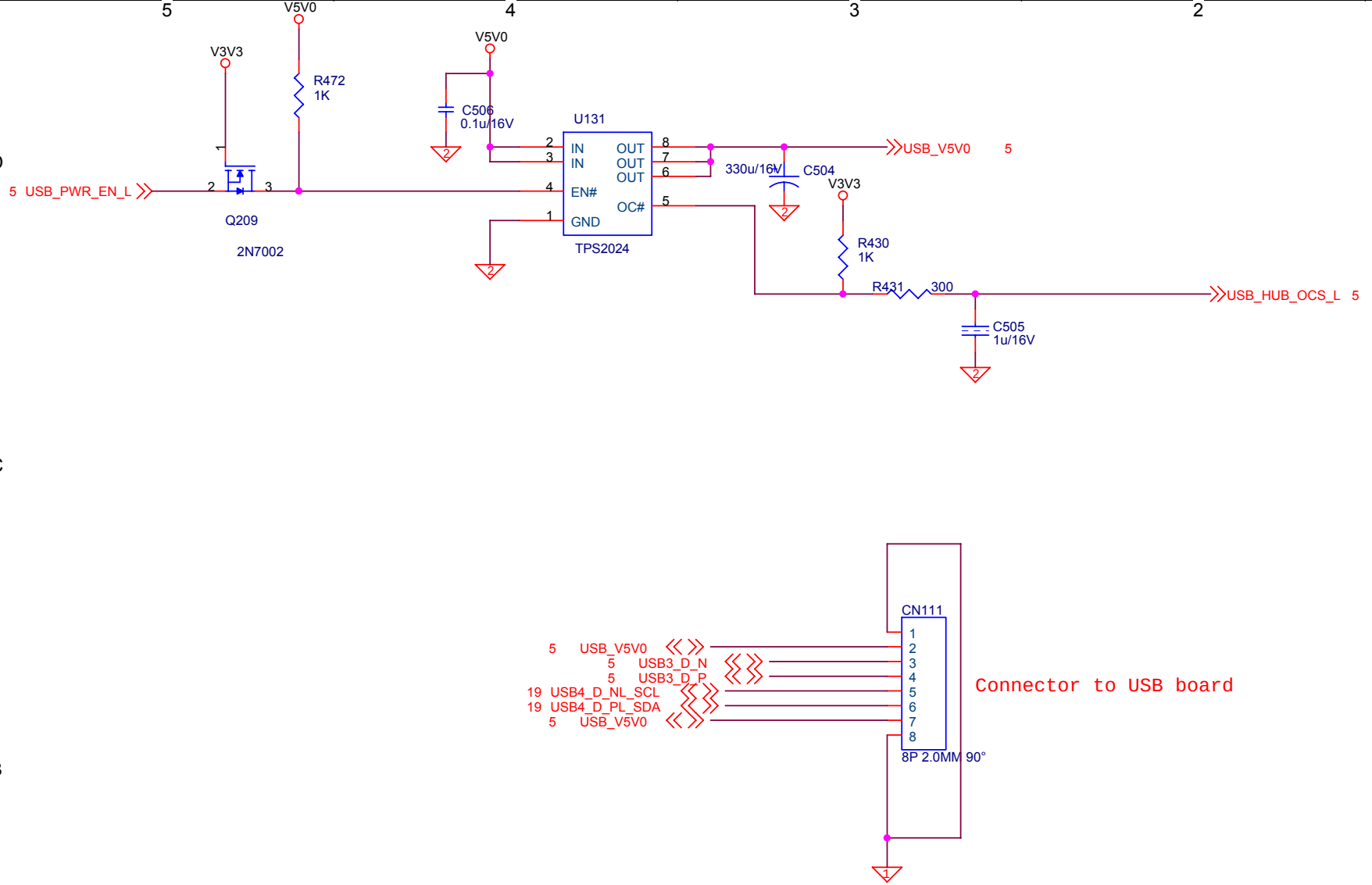
Note5
For 24" or 26" Model.

Note4
FOR B22W

U128
NT68668

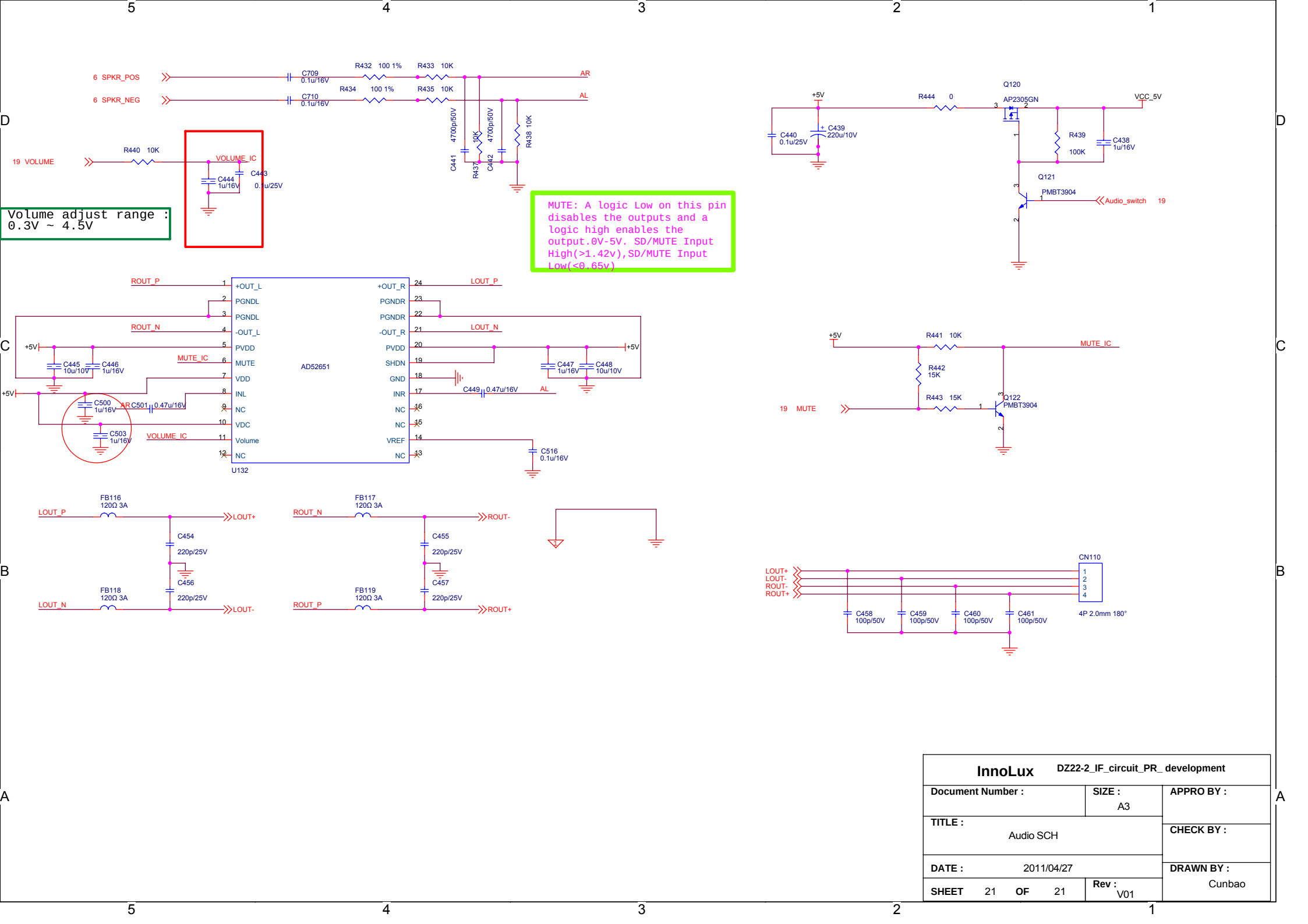
OE	S	HSD1+/HSD1-	HSD2+/HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	X	OFF	OFF

Document Number :	SIZE : A2
TITLE : Scaler	APPRO BY :
DATE : 2011/04/27	CHECK BY :
SHEET 19 OF 21	Rev : V01
InnoLux DZ22-2_IF_circuit_PR_ development	DRAWN BY : Cunbao



Connector to USB board

InnoLux DZ22-2_IF_circuit_PR_ development		
Document Number :	**SIZE :** A4	**APPRO BY :**
TITLE : USB		**CHECK BY :**
DATE : 2011/04/27		**DRAWN BY :** Cunbao
SHEET 20 **OF** 21	**Rev :** V01	



InnoLux	**DZ22-2_IF_circuit_PR_ development**		
Document Number :		**SIZE :** A3	**APPRO BY :**
TITLE : Audio SCH			**CHECK BY :**
DATE : 2011/04/27			**DRAWN BY :** Cunbao
SHEET 21 **OF** 21		**Rev :** V01	